IP 8-Channel Timer Module

Mike Shea and Mike Kucera
September 25, 1994

This note describes an eight channel predet timer, implemented as an IndustryPack™† module, using an Actel-1280 field programmable gate array. The 1280 gate array is a user programmable chip that can be configured and programmed locally in the Actel development system. The Timer Module receives the 10 MHz Tevatron event clock, decodes events, outputs eight programmable delay pulses along with four gate pulses that span the time between pairs of delay pulses. The delayed pulses are referenced to selectable clock events or to external trigger pulses.

Physically, the IndustryPack Module is a 1.8" by 3.9" circuit board that contains two high density 50-pin "D" female connectors as defined by the GreenSpring IndustryPack specification. This specification is a public domain definition of a small mezzanine board for use in microprocessor-based systems. Figure 1 is a diagram of the IP eight channel timer module showing the parts placement including the two 50-pin connectors, one logic interface and one for user I/O signals. The logic interface includes:

D0-D15	16 bit data
IOSEL/	I/O Addr space select
INTSEL/	Interrupt Select
INTREQ0	Interrupt request
ACK/	Acknowledge
R-W/	Read-Write control
Addr 1..6	I/O space Address lines
Reset/	Clears all registers, inhibits triggers (low active)

At the present time, the Actel chip does not assert an interrupt request, but interrupt capability could be added into the Actel design if required. The Actel chip contains the following circuitry:

- IP logic interface
- Four Control/Status register
- Tevatron-style event clock decoder
- Four Trigger event registers
- Six 16-bit delay counter
- Eight 16-bit delay comparators
- Divide by 10 clock prescaler
- Eight delayed trigger output
- Four gate outputs

Two 74F3037 4-bit 50-ohm buffers drive the gate pulses, the reference strobe that triggered the timers, the 10 MHz clock recovered from the input event clock, and two copies of the input clock. A 10 MHz oscillator included on the board can be selected for use as a local timebase.

The input Tevatron clock is received by a discriminator that has a self tracking reference input. This design eliminates the need to adjust the input discriminator level for various amplitude input signals. A second discriminator clamps the output of the first discriminator in the absence of an input signal.

Registers in the Actel part are mapped into the Industry-Pack I/O space. An *IOSEL* is generated by the carrier board to allow word access to the gate array registers. All addresses in this note are offsets from the IP module's base address that is selected by the carrier board. Figure 2 shows the Actel pinout and the register map of the module. Registers in the 8-channel chip are arranged as two sets of registers that are similar to the earlier 4-channel timer design. The chip is initialized by loading the delay values into the first four words, the triggering event into the least significant byte of word addresses $08, $0C, $18, and $1C, and the control register contents into the least significant byte of addresses $0A, $0E, $1A and $1E. Bits in the control register can be set to individually enable the functions shown in Figure 3. These include:

- Enabling the delay timer outputs
- Prescaling the 10 MHz timebase
- Enabling daisychain mode
- Selecting: External 10 MHz timebase
  Event trigger
  Offboard trigger
  Onboard trigger from the 22V10
  Output pulse length

Figure 4 gives the pinout of the 50-pin carrier board connector user connector.

Inside the Actel part, the delay comparators for channels 0,1 compare against a single 16-bit counter; channels 4,5 compare against another 16-bit counter. This is done only because of limitations in the number of available gates. As the counters increment, a match is found and a delayed output pulse is generated. Comparators 2, 3, 6 and 7 compare the stored delay value against four separate counters.

When the daisychain mode is selected, channel 2 and 3 counters are started by the delayed output pulses of channels 0 and 1; channels 6 and 7 counters are started by the delayed output pulses of channels 4 and 5, respectively. This design allows up to four *START and WIDTH* pulse pairs to be generated to control devices

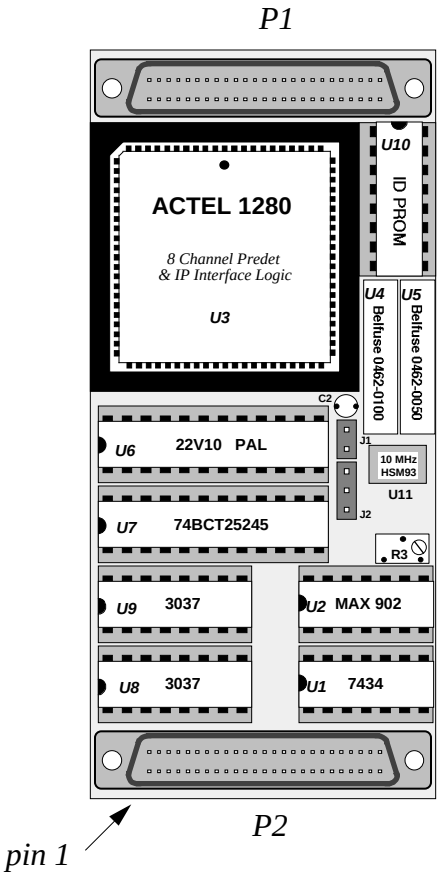
that cannot tolerate receiving an *OFF* pulse before receiving an *ON* pulse. Also, changing the *START* time of such a pair will not change the value of the *WIDTH*. Daisychaining 0 to 2, 1 to 3, 4 to 6, and 5 to7 are controlled by control register bits CR00, CR20, CR40, and CR60, respectively. Functions of all the control register bits are given in Figure 3.

Four gate outputs are generated by the Actel chip. Gate0 is asserted when Trigger0 is output; removed when Trigger2 is output. Similarly, trigger pairs 1-3, 4-6, and 5-7 determine the assertion and removal of Gate1, Gate2, and Gate3, respectively. Note the gate signals are generated as described above whether or not the daisychain mode is selected. In the event that, for example, Trigger2 comes just before Trigger0, the gate0 output will be asserted all the time except for the time betwee Trigger2 and Trigger0.

Although the IP module described here has been designed as a predet timer , the board itself can serve as a platform for testing or building other Actel designs. The basic board provides an Actel chip with an IndustryPack connection to a carrier board, three dedicated external inputs, and two bytes of buffered digital I/O. Data direction of signals to the octal I/O buffer is controlled by an Actel chip output. The 22V10 can be used or bypassed. Using this board, it should be possible to easily implement special devices such as pulse counters, pulse burst generators, and high speed stepping motors.

---

† IndustryPack and IP are trademarks of GreenSpring Computers, Inc.



IPDEL8 Predet Timer

Input: TCLK event clock

Outputs: 8 Delay Timers
4 Variable-width Gates
2 TCLK Signals
1 10 MHz Signal

Figure 1. *Industry Pack*–Based 8-Channel Predet Module

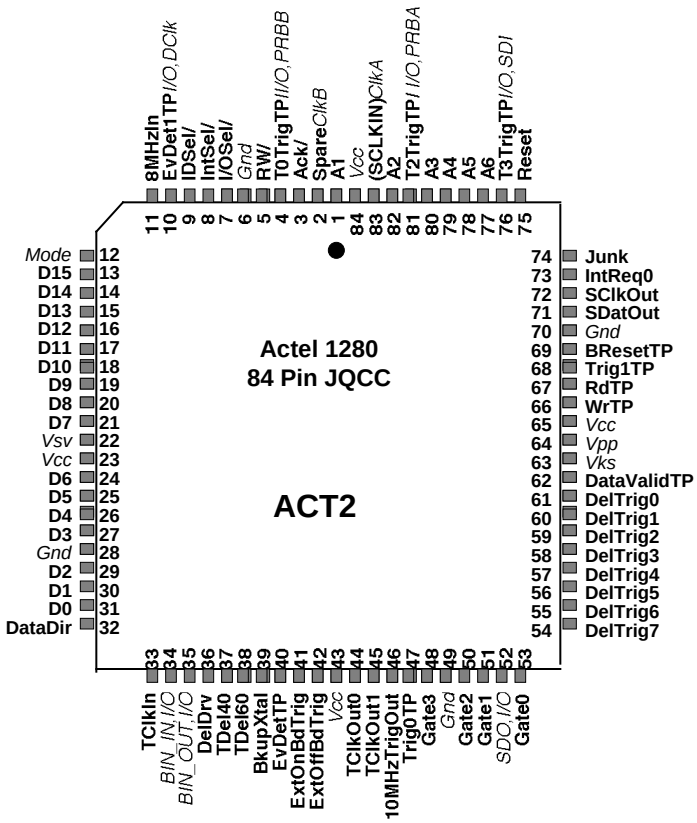


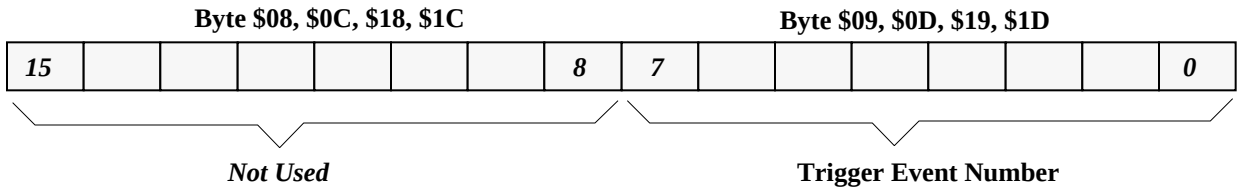
Figure 2a. IP 8 Channel Timer Actel Pinout

Address	R/W	Function
Base + 0	R/W	Channel 0 delay
Base + 2	R/W	Channel 1 delay
Base + 4	R/W	Channel 2 delay
Base + 6	R/W	Channel 3 delay
Base + 8	R/W	Trigger Event 0
Base +A	R/W	Control Register 0
Base + C	R/W	Trigger Event 2
Base + E	R/W	Control Register 2
Base + 10	R/W	Channel 4 delay
Base + 12	R/W	Channel 5 delay
Base + 14	R/W	Channel 6 delay
Base + 16	R/W	Channel 7 delay
Base + 18	R/W	Trigger Event 4
Base + 1A	R/W	Control Register 4
Base + 1C	R/W	Trigger Event 6
Base + 1E	R/W	Control Register 6

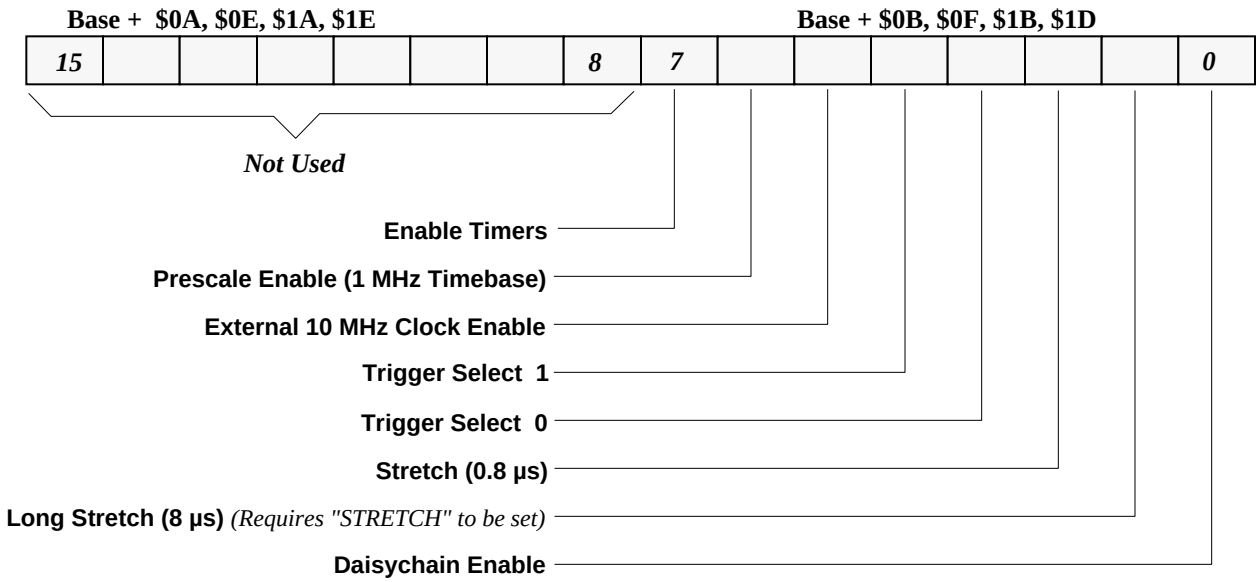
Note: Only Word Accesses are Supported
Trigger Event and Control Registers occupy the low byte

Figure 2b. IP 8 Channel Timer Address Map

Event Register



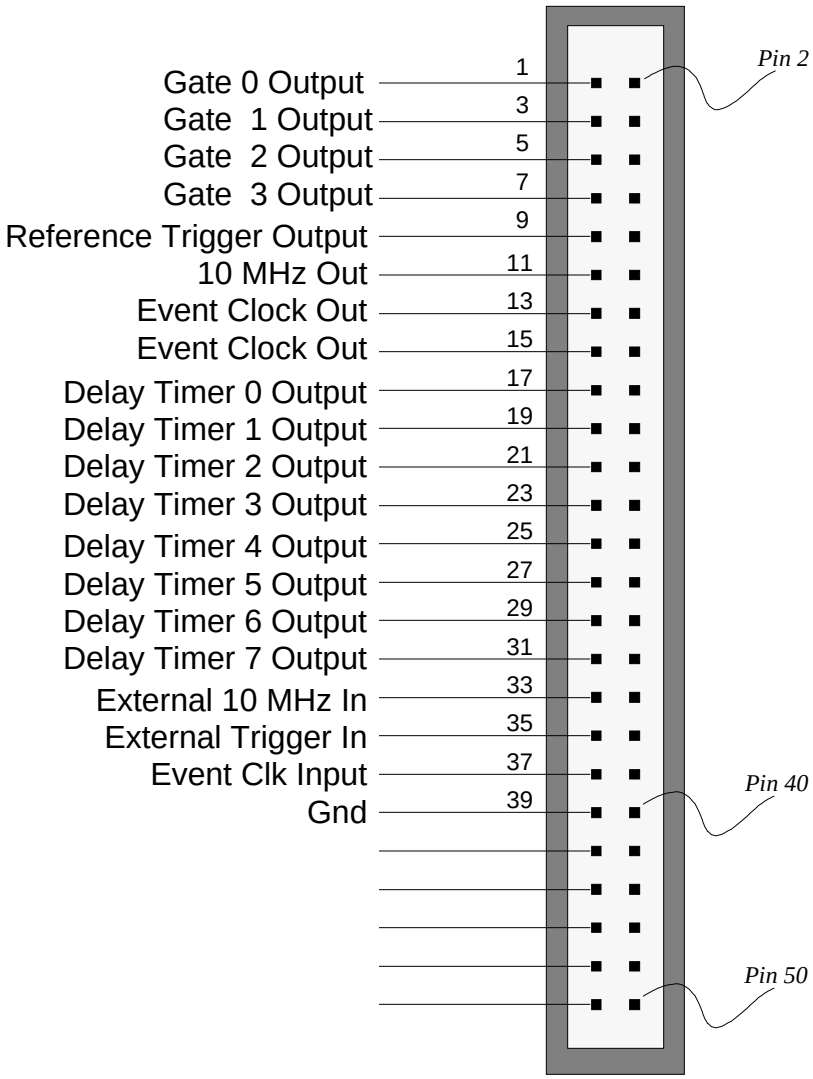
Control Register



Trigger Select	Trigger Source
0 1 2 3	15Hz Reset Event Detect Onboard External Trigger Offboard Extrenal Trigger

Figure 3. Control Registers for IP 8 Channel Timer Gate Array

m/s 092694



Notes: All Even Numbered Pins are Gnd.
Pin numbers of the IP module connector P2 are the same as for Carrier Board connector

Figure 4. IP User Connector Pinout for 8 Channel Timer